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Release Summary

Link™ Capture Software 11.5

This document gives an overview of the functionality of the Link™ Capture Software 11.5 release for the Intel® Programmable Acceleration Card with Intel® Arria® 10 GX FPGA as well as the 2 × 100 Gbit/s, 1 × 100 Gbit/s, 2 × 40 Gbit/s, 8 × 10 Gbit/s, 4 × 10 Gbit/s, 2 × 10 Gbit/s and 4 × 1 Gbit/s NT SmartNICs, NT200A02-2×100/40, NT200A02-2×40/8×10, NT200A02-8×10/2×40, NT200A01-2×100/40, NT200A01-2×100, NT200A01-2×40, NT200A01-8×10/2×40, NT200C01-2×100, NT100E3-1-PTP, NT80E3-2-PTP, NT80E3-2-PTP-8×10/2×40, NT40A01-4×10/1-SLB, NT40E3-4-PTP, NT20E3-PTP, NT40A01-4×1, NT20E2, NT20E2-PTP, NT4E2-4-PTP, NT4E and NT4E-STD.

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Modification History

This document has been updated as follows:

Rev.	Date	Comment
1	2019-04-17	Initial version.

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1 Summary of the Link™ Capture Software 11.5 Release

In this document

This document gives a brief overview of the Link™ Capture Software 11.5 release for the NT SmartNICs as well as the Intel® Programmable Acceleration Card with Intel® Arria® 10 GX FPGA (Intel® PAC with Intel® Arria® 10 GX FPGA or Intel® PAC A10 GX for short).

Note: The Link™ Capture Software 11.5 release supports Napatech SmartNICs with fourth-generation architecture (also referred to as 4GA) as well as Napatech SmartNICs with third-generation architecture (also referred to as 3GA).

Note: If Napatech 3GA and 4GA SmartNICs are combined in the same server, filtering based on port numbers is the only available filtering.

Note: This document only describes the 4GA features. The corresponding document describing the latest 3GA release is DN-0971, Napatech, Green Bay 2, Release Summary.

Terminology

In this document the term NT80E3-2-PTP does not include NT80E3-2-PTP-8×10/2×40 SmartNICs, except in the title of the Hardware Installation Guide (DN-0980), the term NT80E3-2-PTP-NEBS does not include NT80E3-2-PTP-NEBS-8×10/2×40 SmartNICs, except in the title of the Hardware Installation Guide (DN-0981), the term NT20E2 does not include NT20E2-PTP SmartNICs, and the term NT4E does not include NT4E2-4-PTP, NT4E2-4T-BP and NT4E-STD SmartNICs. However, the term NT200C01-2 includes NT200C01-2-NEBS SmartNICs, the term NT100E3-1-PTP includes NT100E3-1-PTP-NEBS SmartNICs, the term NT80E3-2-PTP includes NT80E3-2-PTP-NEBS SmartNICs, the term NT80E3-2-PTP-8×10/2×40 includes NT80E3-2-PTP-NEBS-8×10/2×40 SmartNICs, the term NT40E3-4-PTP includes NT40E3-4-PTP-NEBS SmartNICs, the term NT20E3-2-PTP includes NT20E3-2-PTP-NEBS SmartNICs, and the term NT4E includes NT4E-4-NEBS SmartNICs, except in contexts where the NEBS SmartNICs are also mentioned specifically.

This chapter contains the following sections:

- Contents of the Link™ Capture Software 11.5 Release on page 6
- Napatech Software Suite Features on page 10
- 4GA Feature Overview on page 10
- Software on page 17

1.1 Contents of the Link™ Capture Software 11.5 Release

Hardware platforms

The Link™ Capture Software 11.5 release applies to these hardware platforms:

- Intel® Programmable Acceleration Card with Intel® Arria® 10 GX FPGA
- NT200A02 analysis SmartNICs (4GA)
- NT200A01 analysis SmartNICs (4GA)
- NT200C01 analysis SmartNICs (4GA)
- NT100E3-1-PTP analysis SmartNICs (3GA and 4GA)
- NT80E3-2-PTP analysis SmartNICs (4GA)
- NT80E3-2-PTP-8×10/2×40 analysis SmartNICs (4GA)
- NT40A01 analysis SmartNICs (4GA)
- NT40E3-4-PTP analysis SmartNICs (3GA and 4GA)
- NT20E3-2-PTP analysis SmartNICs (3GA and 4GA)
- NT20E2 capture and in-line SmartNICs (3GA)
- NT20E2-PTP analysis SmartNICs (3GA)
- NT4E2-4-PTP analysis SmartNICs (3GA)
- NT4E capture and in-line SmartNICs (3GA)
- NT4E-STD capture SmartNICs (3GA)

Operating systems

The Link™ Capture Software 11.5 release supports:

- Linux kernel 3.0 to 3.19 and 4.3 to 4.18, 64-bit

  Note: For Intel® PAC with Intel® Arria® 10 GX FPGA only Linux kernel 3.10 through 4.7 are supported.

- Windows Server 2016 and Windows Server 2019, 64-bit

Note: Intel® PAC with Intel® Arria® 10 GX FPGA is only supported for Linux.

Note: NT40A01-4×10/1-SLB SmartNICs are only supported for Linux.

Feature sets

The Link™ Capture Software 11.5 release corresponds to these feature sets:

- 4GA:
  - N-ANL11

    Applies to:

    - NT200C01-2×100
    - NT100E3-1-PTP
    - NT200A02-2×100/40
    - NT200A01-2×100/40 running at 2 × 40 Gbit/s
    - NT200A01-2×40
    - NT80E3-2-PTP
    - NT200A02-2×40/8×10 (**NEW**)
    - NT200A02-8×10/2×40 (**NEW**)
    - NT200A01-8×10/2×40
    - NT80E3-2-PTP-8×10/2×40
    - NT40E3-4-PTP
    - Intel® PAC with Intel® Arria® 10 GX FPGA
    - NT20E3-2-PTP
    - NT40A01-4×1
  - N-ANL10

    Applies to:

    - NT200A01-2×100
    - NT200A01-2×100/40 running at 2 × 100 Gbit/s
    - NT40A01-4×10/1-SLB
- 3GA:
  - N-ANL3A

    Applies to:

    - NT100E3-1-PTP
    - NT40E3-4-PTP
    - NT20E3-2-PTP
  - N-ANL2

    Applies to:

    - NT20E2-PTP
    - NT4E2-4-PTP
  - N-CAP16

    Applies to: NT20E2-CAP
  - N-CAP12A

    Applies to: NT4E-CAP
  - N-INL8

    Applies to: NT20E2-INL
  - N-INL4A

    Applies to: NT4E-INL
  - S-CAP2

Applies to: NT4E-STD-CAP

Note: The `inline` profile is not supported.

The main 4GA features are listed in 4GA Feature Overview on page 10.

New features

These features are new in the Link™ Capture Software 11.5 release:

- Support for NT200A02-2×40/8×10 and NT200A02-8×10/2×40

Napatech Software Suite features

The general features of Napatech Software Suite are described in Napatech Software Suite Features on page 10.

Product packages

The Link™ Capture Software 11.5 release consists of these product packages:

- **ntanl_package_3gd_intel_pac-11.5.x-linux**
- **ntanl_package_3gd-11.5.x-linux**
- **ntanl_package_3gd-11.5.x-windows**

The **ntanl_package_3gd_intel_pac-11.5.x-linux** product package includes two Accelerator Functional Units (AFUs) for the Intel® Programmable Acceleration Card with Intel® Arria® 10 GX FPGA for running at 1 × 40 Gbit/s and at 4 × 10 Gbit/s, respectively, Napatech Software Suite, tools packages, libpcap and documentation for standard use. The software components are described in Software on page 17. FPGA images for the NT SmartNICs supported by the Link™ Capture Software 11.5 release can be found in one of the other product packages for the Link™ Capture Software 11.5 release.

The **ntanl_package_3gd-11.5.x-linux** and **ntanl_package_3gd-11.5.x-windows** product packages include FPGA images for the NT SmartNICs (with **`imgctrl`** tool for upgrading), two Accelerator Functional Units (AFUs) for the Intel® Programmable Acceleration Card with Intel® Arria® 10 GX FPGA for running at 1 × 40 Gbit/s and at 4 × 10 Gbit/s, respectively, Napatech Software Suite, tools packages, libpcap/WinPcap and documentation. The software components are described in Software on page 17.

Included documents

The Link™ Capture Software 11.5 release includes these documents:

Note: All of these documents are not necessarily included in each product package.

Note: The documents can also be found on docs.napatech.com (the Napatech Documentation Portal).

Note: The documents relevant for Napatech 3GA SmartNICs are not included in the product packages for the Link™ Capture Software 11.5 release. They can be found in the corresponding 3GA product packages.

- Napatech, NT 4GA SmartNICs with Napatech Software Suite, Getting Started, Overview Document, DN-0931 (**UPDATED**)
- Napatech, Napatech Link™ Capture Software for Intel® PAC with Intel® Arria® 10 GX FPGA, Installation and Use, Quick Guide, DN-1113 (**UPDATED**)
- Napatech, Using the Napatech Support Portal, User Guide, DN-1118
- Napatech, Link™ Capture Software 11.5, Release Summary, DN-1210 (**NEW**)
- Napatech, Napatech Software Suite, From Green Bay 2 to Link™ Capture Software 11.5, Migration Document, DN-1212 (**NEW**)
- Napatech, Napatech Software Suite, From Link™ Capture Software 11.4 to Link™ Capture Software 11.5, Migration Document, DN-1211 (**NEW**)
- Napatech, NT200A02-SCC, Installation and Specifications, Hardware Installation Guide, DN-1169 (**UPDATED**)
- Napatech, NT200A02-NEBS, Installation and Specifications, Hardware Installation Guide, DN-1200 (**UPDATED**)
- Napatech, NT200A01-SCC, Installation and Specifications, Hardware Installation Guide, DN-1016 (**UPDATED**)
- Napatech, NT200A01-NEBS, Installation and Specifications, Hardware Installation Guide, DN-1017 (**UPDATED**)
- Napatech, NT100E3-1-PTP and NT200C01-SCC, Installation and Specifications, Hardware Installation Guide, DN-0848
- Napatech, NT100E3-1-PTP-NEBS and NT200C01-NEBS, Installation and Specifications, Hardware Installation Guide, DN-0896
- Napatech, NT80E3-2-PTP, Installation and Specifications, Hardware Installation Guide, DN-0980
- Napatech, NT80E3-2-PTP-NEBS, Installation and Specifications, Hardware Installation Guide, DN-0981
- Napatech, NT40A01-SCC, Installation and Specifications, Hardware Installation Guide, DN-0954
- Napatech, NT40A01-NEBS, Installation and Specifications, Hardware Installation Guide, DN-0955
- Napatech, NT40E3-4-PTP, Installation and Specifications, Hardware Installation Guide, DN-0797
- Napatech, NT40E3-4-PTP-NEBS, Installation and Specifications, Hardware Installation Guide, DN-0897
- Napatech, NT20E3-2-PTP, Installation and Specifications, Hardware Installation Guide, DN-0904
- Napatech, NT20E3-2-PTP-NEBS, Installation and Specifications, Hardware Installation Guide, DN-0905
- Napatech, SmartNICs with Napatech Software Suite, Software Installation for Linux, Software Installation Guide, DN-0379
- Napatech, NT SmartNICs with Napatech Software Suite and WinPcap, 4GA Software Installation for Windows, Software Installation Guide, DN-1067
- Napatech, SmartNICs with Napatech Software Suite, libpcap Installation, Software Installation Guide, DN-0428

- Napatech, 4GA SmartNICs with Napatech Software Suite, Software Architecture, Overview Document, DN-0810 (**UPDATED**)
- Napatech, Napatech Software Suite, Reference Documentation, DN-0449 (**UPDATED**)
- Napatech, 4GA SmartNICs with Napatech Software Suite, Time-Stamping and Time Synchronization, User Guide, DN-0985 (**UPDATED**)
- Napatech, 4GA SmartNICs with Napatech Software Suite, Statistics, User Guide, DN-0986
- Napatech, 4GA SmartNICs with Napatech Software Suite, Multi-CPU Distribution, User Guide, DN-0988
- Napatech, NT SmartNICs, Handling FPGA Images, User Guide, DN-0487 (**UPDATED**)
- Napatech, SmartNICs with Napatech Software Suite, Basic Troubleshooting, User Guide, DN-0737
- Napatech, Napatech Software Suite, Running Snort, Application Note, DN-0666
- Napatech, Napatech Software Suite, Opening Multiple Network Streams as One, Application Note, DN-0740
- Napatech, NT SmartNICs with Napatech Software Suite, Qualifying, Fine-Tuning and Troubleshooting Time Synchronization, Application Note, DN-0793
- Napatech, NT80E3-2-PTP, Running at 8 × 10 Gbit/s, Application Note, DN-1133
- Napatech, 4GA SmartNICs with Napatech Software Suite, Feature Set N-ANL11, Feature Description, DN-1128 (**UPDATED**)

1.2 Napatech Software Suite Features

Data sharing

Multiple streams can get access to the same host buffer.

Packet merging

Packets from different host buffers can be merged into one stream based on time stamps. In this way traffic from different SmartNICs can be merged.

Port virtualization

All ports on all SmartNICs are numbered sequentially.

Hardware abstraction

HAL (hardware abstraction layer) macros are provided for all hardware-generated information in the standard packet descriptor and in extended descriptor 9.

1.3 4GA Feature Overview

In this section

This section gives an overview of the 4GA features in the Link™ Capture Software 11.5 release.

Packet descriptors

These packet descriptors are available:

- Standard packet descriptor
- Dynamic packet descriptor 1
- Dynamic packet descriptor 2
- Dynamic packet descriptor 3
- Dynamic packet descriptor 4
- PCAP packet descriptor

Packet descriptor extension

For frames with a standard packet descriptor, extended packet descriptor 9 is available.

Statistics counters per port

RMON1 and extended RMON1 statistics counters are available for each port.

Statistics counters per color

These statistics counters are available for each color:

- Frame counters
- Byte counters

Statistics counters per stream ID

These statistics counters are available for each stream ID:

- Frame counters for forwarded frames
- Frame counters for flushed frames
- Frame counters for dropped frames
- Byte counters for forwarded frames
- Byte counters for flushed frames
- Byte counters for dropped frames

Port merging

Frames from multiple ports on the same SmartNIC can be merged into one stream.

QPI bypass

When two NT100E3-1-PTP SmartNICs are connected and working as an NT200C01 solution, it is possible to transfer data received on one NT100E3-1-PTP SmartNIC via the interconnect cable to the other NT100E3-1-PTP SmartNIC and vice versa. In this way data destined for a specific NUMA node can be delivered over the PCIe bus of the SmartNIC that is local to this NUMA node and thereby the QPI in the host can be bypassed to avoid introducing additional latency.

CPU socket load-balancing

Two NT40A01-4×10/1-SLB SmartNICs can be bonded in a master/slave configuration so that all traffic received on the master SmartNIC is replicated to the slave SmartNIC, ensuring local cache access to two NUMA nodes in a dual-CPU-socket server to optimize performance.

Time stamp formats

Received frames are time-stamped according to the internal SmartNIC time either when the first byte is received or when the last byte is received.

Note: Start-of-frame time-stamping does not apply to NT40E3-4-PTP SmartNICs nor to the Intel® Programmable Acceleration Card with Intel® Arria® 10 GX FPGA.

These time stamp formats are available:

- PCAP-ns format, 1 ns (only if PCAP packet descriptor is selected)
- Native UNIX format, 1 ns
- Native UNIX format, 10 ns
- PCAP-µs format, 1000 ns (only if PCAP packet descriptor is selected)

All received frames use the same time stamp format. Offset compensation is available.

RX data path delay values are available in the API to allow applications to compensate for these delays.

Time stamp synchronization

An Intel® Programmable Acceleration Card with Intel® Arria® 10 GX FPGA can be synchronized to OS time with dynamic drift adjustment.

Two or more NT SmartNICs can be synchronized, one being the master and the other(s) being slaves connected using daisy chain.

When configured as master and connected to another NT SmartNIC, an NT SmartNIC can provide a synchronized set of external time and SmartNIC time every second. The external time is the time of the other SmartNIC. Synchronized sets of external time and SmartNIC time can also be obtained every 20 µs.

When an NT SmartNIC is configured as master and connected to a time device, for instance a GPS, the PPS signal from the time device can trigger the sampling of the SmartNIC time.

The NT SmartNIC time stamp clock rate can be synchronized relative to any external time source with a PPS output at TTL levels. If absolute time information is available, the SmartNIC time clock can be synchronized to the absolute UTC time.

Minor adjustments to the internal NT SmartNIC time can be done using a sliding adjust; and cable delays can be compensated for.

When two or more NT SmartNICs are synchronized with respect to absolute time, block statistics are transferred synchronously from the SmartNICs to the host.

For all time reference sources (with OS, NT-TS, PPS or PTP time synchronization) the same time synchronization statistics are supported for NT SmartNICs:

- Current offset to master
- Mean value
- Minimum and maximum offset to master
- Peak-to-peak jitter
- Calculated mean offset to master
- Calculated standard deviation
- Time since last reset of statistics calculation

IEEE 1588-2008 PTP v2 clock synchronization

The IEEE 1588-2008 PTP v2 clock synchronization functionality allows the SmartNICs to be synchronized against a PTP grandmaster, using the PTP Ethernet port on the SmartNIC.

Note: IEEE 1588-2008 PTP v2 clock synchronization does not apply to the Intel® Programmable Acceleration Card with Intel® Arria® 10 GX FPGA.

These PTP Ethernet port configurations are supported: Static IP, DHCP and VLAN.

These communication protocols are supported: IPv4/UDP and IEEE802.3 (layer2).

These PTP profiles are supported: PTP Default and Telecom.

The SmartNICs support both end-to-end (delay request-response mechanism) and peer-to-peer (peer delay mechanism) for propagation delay measurements.

SyncE support

NT SmartNICs can utilize SyncE-enabled networks to provide highly stable frequency synchronization.

Note: SyncE does not apply to NT200A02 and NT200A01 SmartNICs nor to the Intel® Programmable Acceleration Card with Intel® Arria® 10 GX FPGA.

Frame classification

Frames are inspected and classified by the frame decoder. These protocols are identified for the different layers:

- Layer 2: ISL encapsulation, VLAN tags, MPLS encapsulation, VN-Tag classification (not for NT40E3-4-PTP nor for Intel® PAC A10 GX)
- Layer 2: EtherII, Novell_RAW, SNAP, LLC, others
- Layer 3: IPv4, IPv6, others
- Layer 4: TCP, UDP, ICMP, SCTP, others
- Tunnel type: GTPv0-U, GTPv1-C, GTPv2-C, GTPv1-U, GRE_v0 (including NVGRE), GRE_v1, IPinIP, EtherIP, VXLAN, others
- Inner layer 2: VLAN tags, MPLS encapsulation
- Inner layer 3: IPv4, IPv6, others
- Inner layer 4: TCP, UDP, ICMP, GRE_v0, SCTP, others

Frames can also be classified as small, large or jumbo frames.

Note: IPv6 is generally supported to the same level as IPv4. In addition, the frame decoder supports a broad range of IPv6 extension headers, as well as filtering based on IPv6 addresses.

IP fragment handling

The IP fragment handling functionality accelerates the processing of fragmented IP traffic and enables the use of 5-tuple (or other non 2-tuple) hash keys on fragments for better CPU load distribution.

Note: IP fragment handling does not apply to NT200A01-2×100 SmartNICs nor to NT200A01-2×100/40 running at 2 × 100 Gbit/s.

Correlation of Packets

Correlation keys can be generated to enable quality of service measurements between multiple points in a network and to accelerate packet deduplication in application software.

Note: Correlation of packets does not apply to NT200A01-2×100/40 running at 2 × 100 Gbit/s, NT200A01-2×100 nor NT40A01-4×10/1-SLB.

Hash value generation

Hash values can be generated from many types of hash keys based on packet header information:

- Last MPLS label
- All MPLS labels
- 2-tuple
- 2-tuple, sorted
- Last VLAN ID
- All VLAN IDs
- 5-tuple
- 5-tuple, sorted
- 3-tuple GREv0
- 3-tuple GREv0, sorted
- 5-tuple SCTP
- 5-tuple SCTP, sorted
- 3-tuple GTPv0
- 3-tuple GTPv0, sorted
- 3-tuple GTPv1 or GTPv2
- 3-tuple GTPv1 or GTPv2, sorted
- Inner 2-tuple
- Inner 2-tuple, sorted
- Inner 5-tuple
- Inner 5-tuple, sorted
- IP fragment tuple
- Round-robin

Hash keys can be selected dynamically for different types of frames.

Source and destination addresses and ports can be swapped in hash calculations. Hash swapping can be based on inner and/or outer IP match lists specifying certain IP addresses.

Multi-CPU distribution (see Multi-CPU distribution on page 15) can be controlled using hash key masks. Hash word bits that are masked out are set to 0. In this way certain parts of the input data can be disregarded from the hash calculation, so that frames with hash values that only differ due to, for instance, port numbers can be configured to end up in the same host buffer.

Filtering

Filtering can be based on:

- Port numbers
- Pattern compares
- Protocol information
- Frame size tests
- Frame error tests
- IP address matching including address groups and wildcard matches
- User-defined key tests that include arbitrary fields

Overlapping filters can be prioritized.

Filtering on tunneled IP traffic is available for GTPv0-U, GRE_v0, IPinIP and EtherIP tunnels.

Packet Coloring

The packet coloring functionality enables tagging of captured frames with a color ID based on the filter logic. The color ID can contain contributions from one filter with the highest priority (color) and/or contributions from a number of filters that the frame matches (color mask). Packet coloring can be used, for instance, in connection with multi-CPU distribution (see Multi-CPU distribution on page 15).

Slicing

Slicing can be both dynamic and fixed, or disabled. These slicing modes are available:

- Fixed length
- Fixed length + ISL
- Fixed length + ISL + ETH + VLAN
- Fixed length + ISL + ETH + VLAN + MPLS
- Fixed length + ISL + ETH + VLAN + MPLS + L3
- Fixed length + ISL + ETH + VLAN + MPLS + L3 + L4
- Fixed length + ISL + ETH + VLAN + MPLS + L3 + L4 + outer data type
- Fixed length + ISL + ETH + VLAN + MPLS + L3 + L4 + outer data type + inner L3
- Fixed length + ISL + ETH + VLAN + MPLS + L3 + L4 + outer data type + inner L3 + inner L4
- End of frame

The end-of-frame dynamic offset enables bytes to be sliced off from the end of the frame by applying a negative offset. This can be used, for instance, for frame checksum removal.

Local retransmission

The local retransmission functionality enables frames received on one network port to be retransmitted to the same port or to another network port on the same SmartNIC without involving the host CPU. The retransmitted frames can be expanded to include a trailer containing a 64-bit RX time stamp with a resolution of 1 ns.

Note: Local retransmission does not apply to NT200A01-2×100 nor to NT200A01-2×100/40 running at 2 × 100 Gbit/s.

Line loopback

Frames received on one network port can be retransmitted to the same network port without involving the host CPU. The line loopback functionality and the filtering/capturing functionality can be used independently of each other.

Host-based transmission

The full host-based transmission functionality enables high-speed transmission with low CPU load of frames located in a host buffer in the server application memory. Frames that have been received by a SmartNIC can be retransmitted by the same or a different SmartNIC without modification.

Note: The full host-based transmission functionality does not apply to NT200A01-2×100 running on the capture image.

Transmission can be both static to a single port and dynamic, where the application can assign different TX ports for different frames.

User data, such as VLAN tags can be inserted into the transmitted frames using dynamic descriptor 3.

Transmission can be timed so that frames are transmitted at specific points in time. In this way frames can be transmitted, for instance, according to their RX time stamps, so that they are replayed as captured. Timed transmission also allows synchronized replay of traffic from a number of different SmartNICs when their time stamp clocks are synchronized.

Limited host-based transmission

Limited host-based transmission only applies to NT200A01-2×100 running on the capture image. This host-based transmission is very CPU-intensive and has a very limited TX rate.

Multi-CPU distribution

Multi-CPU distribution enables the SmartNIC to off-load the CPU load-balancing by distributing the processing of captured frames in the host CPU. Data can be placed in separate buffers based on port numbers, hash values and filtering.

Buffer system

The buffer system supports the use of up to 128 RX buffers per SmartNIC in host memory with dynamic host buffer segment size and up to 64 RX buffers with static host buffer segment size.

Note: Dynamic segment size does not apply to the Intel® Programmable Acceleration Card with Intel® Arria® 10 GX FPGA.

1.4 Software

Software APIs

These software APIs are included:

- NTAPI (Napatech application programming interface)

  Napatech application programming interface is a stream-based, packet- or segment-based zero-copy API. User space libraries are included in binary, and the kernel space driver is included as open source (GPL-compliant).

- NTPL (Napatech programming language)

  Napatech programming language is a highly efficient interface, which optimizes the use of the FPGA resources. In the Link™ Capture Software 11.5 release these functions are supported:

  - Dynamic packet descriptors
  - Filtering
  - Slicing
  - Hash key definition
  - Multi-CPU distribution
  - Correlation key (does not apply to NT200A01-2×100 nor to NT200A01-2×100/40 running at 2 × 100 Gbit/s)
  - Local retransmission (does not apply to NT200A01-2×100 nor to NT200A01-2×100/40 running at 2 × 100 Gbit/s)
  - IP fragment handling (does not apply to NT200A01-2×100 nor to NT200A01-2×100/40 running at 2 × 100 Gbit/s)

- libpcap

  A libpcap source library is available for integration of libpcap applications.

- WinPcap

  A WinPcap source library is available for integration of WinPcap applications.

Tools

The Link™ Capture Software 11.5 release includes a tools package with a number of binary tools that demonstrate the SmartNIC functionality. These tools are included:

- `adapterinfo` (displays information about the SmartNIC)
- `capfileconvert` (converts captured files to or from 3GD (Napatech Software Suite) format)
- `capfiledump` (dumps a 3GD (Napatech Software Suite) capture file in humanly readable format)
- `capture` (captures data to disk – only applies to SmartNICs with a capture profile)
- `config` (configures links, time stamp values and sensor alarm levels)
- `diagnostics` (perform diagnostics on a SmartNIC)
- `latency` (not used)
- `monitoring` (queries the system port statistics)
- `nimconfig` (reads/writes values from/to the memory of network interface modules)
- `ntinfo` (collects information about the host buffer utilization once per second, and creates a host buffer utilization report)
- `ntlog` (reads out the driver log)
- `ntpcap_capture` (captures data received from a PCAP interface and stores it to disc in true PCAP file format.)
- `ntpcap_replay` (replays any captured PCAP or PCAPNG file)
- `ntpl` (sends NTPL code to a certain network stream)
- `osmode` (creates a virtual network device on top of 3GD (Napatech Software Suite))
- `pktgen` (performs traffic generation – does not apply to NT200A01-2×100 running on the capture image)
- `pps_basic` (synchronizes the SmartNIC against a PPS signal – does not apply to Intel® PAC with Intel® Arria® 10 GX FPGA)
- `pps_endrun` (synchronizes the SmartNIC against a PPS signal from an EndRun Præcis Cf CDMA receiver or an EndRun Præcis II CDMA receiver – does not apply to Intel® PAC with Intel® Arria® 10 GX FPGA)
- `pps_oregano` (synchronizes the SmartNIC against a PPS signal from an Oregano SYN1588 PCIe NIC – does not apply to Intel® PAC with Intel® Arria® 10 GX FPGA)
- `pps_os` (synchronizes the SmartNIC against a PPS signal using OS time as input – does not apply to Intel® PAC with Intel® Arria® 10 GX FPGA)
- `pps_ptp` (enables PPS on all SmartNICs configured to run PPS – does not apply to Intel® PAC with Intel® Arria® 10 GX FPGA)
- `pps_symmetricom` (synchronizes the SmartNIC against a PPS signal from a Microsemi SyncServer® – does not apply to Intel® PAC with Intel® Arria® 10 GX FPGA)
- `productinfo` (displays product information about a SmartNIC)
- `profiling` (queries the system for profiling data)
- `ptp_port_config` (reads/writes values of selected PTP port parameters – does not apply to Intel® PAC with Intel® Arria® 10 GX FPGA)
- `readproperty` (queries the properties of the Napatech Software Suite)
- `replay` (transmits a file with captured traffic – does not apply to NT200A01-2×100 running on the capture image)
- `supportinfo` (dumps system information for support purposes)
- `throughput` (captures to server memory and shows the throughput)
- `vpd` (reads/writes VPD (vital product data) user data)

Examples

The Link™ Capture Software 11.5 release includes an examples package for the SmartNICs with a number of code examples that use the SmartNIC functionality to illustrate how user applications can be made. These examples are included:

- `bypass/config` (not used)
- `bypass/info` (not used)
- `bypass/watchdog` (not used)
- `config` (is an example of how to use the configuration stream interface in NTAPI)
- `event` (is an example of how to use the event stream interface in NTAPI)
- `eventMonitor` (is an example of how to monitor events and dump information about them to the screen using the event stream interface in NTAPI)
- `hashref/calc_single_hash` (is an example of how to use the hash reference library to calculate hash values for some variants of key data)
- `info` (is an example of how to use the information stream interface in NTAPI)
- `integration/systemd` (contains a unit configuration for systemd)
- `integration/sysv` (contains a System V **`init`** script enabling **`ntservice`** to be started and stopped by a System V compatible **`init`** process)
- `integration/upstart` (contains a job file for **`Upstart`**, enabling **`ntservice`** to be controlled by **`Upstart`**)
- `net/addPacket` (is a legacy example of how to implement a simple VLAN tagging, using limited host-based transmission - only applies to NT100E3-1-PTP and NT40E3-4-PTP)
- `net/analysis` (is an example of how to perform real-time analysis of packets using the file network stream interface in NTAPI)
- `net/capfileconvert` (is an example of how to convert captured files)
- `net/capture` (is an example of how to capture to disk using the RX network stream interface in NTAPI)
- `net/inline` (not used)
- `net/ipfdemo` (is an example of how to use IP fragment handling – does not apply to NT200A01-2×100 nor to NT200A01-2×100/40 running at 2 × 100 Gbit/s)
- `net/netflow` (is an example of how to use the dynamic descriptor 1 to extract net flow information from a packet)
- `net/numa` (is an example of how to assign and use a host buffer on a NUMA mode)
- `net/readcapfile` (is an example of how to read a capture file using NTAPI)
- `net/replay` (not used)
- `net/replay4GA` (is an example of how to replay captured data onto a port using the TX network stream interface in NTAPI – does not apply to NT200A01-2×100 running on the capture image)
- `net/replayGS` (not used)
- `net/streamidstatistics` (is an example of how to get stream ID statistics that can be correlated with what the application receives)
- `net/transmit_multifunction` (is an example of how to transmit different packet sizes at different rates on different ports by transmitting data in segments using NTAPI)
- `net/transmit_on_timestamp` (is an example of how to transmit packets on time stamp using the packet interface in NTAPI)
- `net/transmit_on_timestamp_setclock` (is an example of how to transmit a sequence of packets on time stamp multiple times using **`TXSETCLOCK`** to advance the delta with the duration of a single replay iteration)
- `net/transmit_packet` (is an example of how to transmit packets using the packet interface in NTAPI)
- `net/transmit_pcap` (is an example of how to transmit PCAP packets using the packet interface in NTAPI)
- `net/transmit_segment` (is an example of how to transmit segments using the TX network stream interface in NTAPI)

- `net/vlandemo` (is an example of how to implement a simple VLAN tagging, using dynamic descriptor 3 and the in-line transmission capabilities – does not apply to Intel® PAC with Intel® Arria® 10 GX FPGA)
- `pps` (is an example of how to use PPS time synchronization – does not apply to Intel® PAC with Intel® Arria® 10 GX FPGA)
- `sensor` (is an example of how to read sensors)
- `stat` (is an example of how to use the statistics stream interface in NTAPI)
- `statUsage` (is an example of how to use the statistics stream interface in NTAPI to read host buffer usage statistics)